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| APPLICATION NO.              | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|------------------------------|-------------|----------------------|---------------------|------------------|
| 10/683,782                   | 10/10/2003  | Shin-Ae Lee          | 5649-1187           | 1793             |
| 20792                        | 7590        | 06/27/2005           | EXAMINER            |                  |
| MYERS BIGEL SIBLEY & SAJOVEC |             |                      | CHEN, JACK S J      |                  |
| PO BOX 37428                 |             |                      | ART UNIT            |                  |
| RALEIGH, NC 27627            |             |                      | PAPER NUMBER        |                  |
|                              |             |                      | 2813                |                  |
| DATE MAILED: 06/27/2005      |             |                      |                     |                  |

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

Application No.

10/683,782

Applicant(s)

LEE ET AL.

Examiner

Jack Chen

Art Unit

2813

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 11 April 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-22 is/are pending in the application.
- 4a) Of the above claim(s) 10, 11 and 13-22 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-9 and 12 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
- 1) ☒ Certified copies of the priority documents have been received.
  - 2) ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - 3) ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date 2/23/04; 2/16/05
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_

### **DETAILED ACTION**

Applicant's election with traverse of the invention of Group II, Species I, with claims 1-9, 12-17 and 20-22 indicated by Applicant to read thereon, in the reply filed on 11 April 2005 is acknowledged. The traversal is on the ground(s) that the species identified in the previous office action did not comprise separate and distinct species and that numerous generic claimed have already been presented. This is not found persuasive because each of the species identified in the previous office is patentably distinct species [i.e., a MOS (PMOS or NMOS) is different from CMOS (having both NMOS and PMOS), in this case, fig. 8 is drawn to a MOS and fig. 20 is drawn to a CMOS] and there is no generic claim. Furthermore, claim 13 does not include/recite all of the claimed limitation/features of claim 1 (i.e., the first LDD under the first lateral protrusion and the second LDD is adjacent to the first LDD, etc.). Further in this regard, the subcombinations are not generic to the combination using the subcombination. (See MPEP 806.04 (c)) Accordingly, the addition of steps or features creates a subcombination-combination relationship, preventing the independent claim from being generic. See MPEP 806.04 (c) and 806.04(d) for the definition of a generic claim.

The requirement is still deemed proper and is therefore made FINAL.

Claims 10-11, 13-22 are withdrawn from further consideration pursuant to 37 CFR 1.142(b), as being drawn to a nonelected species, there being no allowable generic or linking claim.

### ***Priority***

Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

***Information Disclosure Statement***

The information disclosure statement filed on February 23, 2004 and February 16, 2005 have been considered.

The listing of references in the specification is not a proper information disclosure statement. 37 CFR 1.98(b) requires a list of all patents, publications, or other information submitted for consideration by the Office, and MPEP § 609 A(1) states, "the list may not be incorporated into the specification but must be submitted in a separate paper." Therefore, unless the references have been cited by the examiner on form PTO-892, they have not been considered.

***Oath/Declaration***

Oath/Declaration filed on October 10, 2003 has been considered.

***Specification***

The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

***Claim Rejections - 35 USC § 102***

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-7, 9 and 12 are rejected under 35 U.S.C. 102(b) as being anticipated by Liou et al., U.S./5,162,884.

Liou et al. disclose a MOS transistor comprising: a gate electrode 8/10 on a substrate 2 (fig. 3d), the gate electrode having a first lateral protrusion 8 extending from a lower portion of a first sidewall of the gate electrode and a second lateral protrusion 8 extending from a lower portion of a second sidewall of the gate electrode (fig. 3d); a drain region 11/15/13 in the substrate comprising a first lightly-doped drain region 13 under the first lateral protrusion (fig. 3d), a second lightly-doped drain region 15 that is deeper than the first lightly-doped drain region 13 adjacent the first lightly-doped drain region (fig. 3d), and a heavily-doped drain region 11 adjacent to the second lightly-doped drain region 15 (fig. 3d); and a source region 11/15/13 in the substrate comprising a first lightly-doped source region 13 under the second lateral protrusion (fig. 3d), a second lightly-doped source region 15 that is deeper than the first lightly-doped source region 13 adjacent the first lightly-doped source region (fig. 3d), and a heavily-doped source region 11 adjacent to the second lightly-doped source region 15 (fig. 3d), see figs. 1-4d and cols. 1-14 for more details.

Re claim 2, further comprising an insulating gate spacer 16 covering the first and second sidewalls of the gate electrode, wherein the second lightly-doped drain region 15 and the second lightly-doped source region 15 are under bottom portions of the insulating gate spacer 16 (fig. 3d).

Re claim 3, wherein the heavily doped drain region 11 is adjacent a first outer sidewall of the insulating gate spacer 16 and wherein the heavily doped source region 11 is adjacent a second outer sidewall of the insulating gate spacer 16 (fig. 3d).

Re claim 4, wherein the gate electrode 8/10 has an inverted T-shape. (fig. 3d)

Re claim 5, further comprising a gate dielectric layer 6 interposed between the gate electrode and the substrate 2 (fig. 3a and 3d).

Re claim 6, further comprising a curing thermal oxide layer 12 on the sidewalls of the gate electrode, the second lightly-doped drain region 15 and the second lightly-doped source region 15 (fig. 3d).

Re claim 7, wherein the insulating gate spacer 16 is on the curing thermal oxide layer 12 (fig. 3d).

Re claim 9, wherein the sidewalls of the first and second lateral protrusions are vertically profiled (fig. 3d).

Re claim 12, further comprising a metal silicide layer 22 on the upper surface of the gate electrode, the surface of the heavily-doped drain region 11 and the surface of the heavily-doped source region 11 (fig. 3d).

### ***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Liou et al., U.S./5,162,884 in view of Lee et al, U.S./5,468,665.

Liou et al. disclosed above; however, Liou et al. are silent to further providing a spacer etch stop layer between spacer and the oxide layer.

Lee et al. teach a semiconductor device, which comprises providing a spacer etch stop layer 777 between spacer 75 and the oxide layer 72 (fig. 7B) in order to protect the substrate during the step of forming the spacer (and an excessive etch of the substrate and contamination of the etchant with plasma species are prevented), see figs. 1A-10E and cols. 1-14 for more details.

Therefore, the subject matter as a whole would have been obvious to one having ordinary skill in the art at the time the invention was made to further providing a spacer etch stop layer between spacer and the oxide layer as taught by Lee et al. in the device of Liou et al. in order to protect the substrate during the step of forming the spacer and prevent excessive etch of the substrate and contamination (see Lee, et al., col. 5, lines 25-32). Moreover, it is noted that the

Art Unit: 2813

spacer etch stop layer is optional as shown in page 10, lines 32-33 and page 18, lines 20-22 of applicant's disclosure.

Furthermore, the specification contains no disclosure of either the critical nature of the claimed process/arrangement (i.e. providing the spacer etch stop layer between the spacer and the oxide layer) or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen limitations or upon another variable recited in a claim, the Applicant must show that the chosen limitations are critical. *In re Woodruff*, 919 F.2d 1575, 1578 (Fed. Cir. 1990).

### ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jack Chen whose telephone number is (571)272-1689. The examiner can normally be reached on Monday-Friday (9:00am-6:30pm) alternate Monday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl W. Whitehead can be reached on (571)272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.



Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Jack Chen  
Primary Examiner  
Art Unit 2813

June 17, 2005